

# Index

## Symbols

- ! (negation) 174
- != (inequality) 174
- !== (not identical) 174
- # delay 166, 216
  - not in analog process 196
- \$abstime 83, 175
- \$bound\_step 77, 190
- \$discontinuity 69, 79, 80, 191
- \$display 192
- \$driver\_... functions 144, 145
- \$fclose 193
- \$fdisplay 193
- \$finish 191
- \$fopen 193
- \$fstrobe 194
- \$limexp 57, 188
- \$monitor 193
- \$random 194
- \$rdist\_... functions 194
- \$realtime 176
- \$stop 191
- \$strobe 84, 192
- \$temperature 57, 177
- \$vt 57, 177
- \$write 193
- % (modulus) 173
- & (bitwise and) 173
- && (logical and) 174
- (—\$—p—) (cross reference) 35
- \* (multiplication) 173
- + (addition) 173
- .model 238, 241, 244
- .subckt 238, 245
- / (division) 173
- < (less than) 174
- << (shift left) 174
- <= (less than or equal to) 174
- == (equality) 174
- ==== (identical) 174
- > (greater than) 174
- > (trigger named event) 174, 217
- >= (greater than or equal to) 174
- >> (shift right) 174
- ? : (inline conditional) 174, 200
- @ event 216
  - different in analog process 196
  - restrictions 178
- ^ (bitwise exclusive or) 173
- ~^ (bitwise exclusive nor) 173
- \_ (in numbers) 153
  - \_VAMS\_ENABLE\_ 151
- {,} concatenate and replicate 154
- | (bitwise or) 173
- || (logical or) 174
- ~ (bitwise invert) 173
- ~& (bitwise nand) 173
- ~^ (bitwise exclusive nor) 173
- ~| (bitwise nor) 173
- 'default\_transition 80, 180
- 'define 151
- 'ifdef 151
- 'include 36, 151
- 'M\_... (math constant) 65, 153
- 'P\_... (physical constant) 65, 153
- 'resetall 152
- 'timescale 152
- 'undef 151
- 'b binary constant 153
- 'd decimal constant 153
- 'h hexadecimal constant 153
- 'o octal constant 153

## A

- a (atto) 154
- above event 120, 207
- restrictions 178

absdelay filter 181  
 absolute tolerance (abstol) 52, 72, 95, 159,  
     162, 168  
 abstime function 83, 175  
 AC analysis 66, 177, 189  
 ac\_stim stimulus 66, 189  
 Acceleration nature 159  
 access function 38, 52, 159, 168  
 access on demand  
     analog values in discrete process 118, 225  
     discrete values in analog process 115, 223  
 ADC model 84, 118  
 always process 103, 209  
 AMS Designer ix, x  
     compatibility 248–258  
 analog event 67, 72, 78, 204  
     restrictions 178  
 analog functions 204  
 analog operators 177  
     restrictions 177, 178  
 analog process 38, 196  
     accessing discrete values 115, 223  
     sensitive to discrete events 115, 225  
     variable capture 57, 114, 198, 223  
     versus event-driven processes 199  
 analog to digital connect module 131  
 analog to digital converter model 84, 118  
 analysis  
     AC 66, 189  
     noise 66, 189  
     small signal 65  
     transient 242  
 analysis function 175  
 angle natures 159  
 arithmetic operators 173  
 array 157  
     bit select 105, 157, 166  
     branch 167  
     constants 154  
     instance 229  
     net 164  
     part select 157, 166  
     port 84, 166  
     see bus  
 assignment 59, 198  
     blocking 107, 213  
     continuous 102, 213  
     delayed 109, 219  
     contribution 38, 60, 169, 198  
     delayed 107, 218  
         continuous 109, 219  
     discrete event 212  
     indirect 170, 172  
         multiple 171  
     net 214  
     non-blocking 108, 213  
     procedural 212, 213  
         continuous 214  
     register 212, 214  
     wreal 111  
 associated reference directions 50  
 autonomous events 78, 206

**B**

barrier model 71  
 base nature 53  
 begin-end block 106, 196, 209  
 behavioral description 227  
 behavioral module 45  
 bi-directional connect module 135  
 binary constant 153  
 bit select 105, 157, 166  
 bit stream generator model 206  
 bit variable 103, 156  
 bitwise operators 173  
 block  
     concurrent 106, 211  
     disable 210  
     named 197, 210  
     parallel, see concurrent block  
     procedural 106, 196, 209  
     sequential, see procedural block  
 blocking assignment 107, 213  
 bottom-up design methodology 17  
 bottom-up verification 28  
 bound\_step function 77, 190  
 branch 47, 167  
     declaration 56, 167  
     named or explicit 56, 167  
     port 168  
     probe 61  
     signal access 168  
     source 62  
     switch 62  
     unnamed or implicit 38, 167  
     vector 167

breakdown warning model 208  
bus 84, 102, 105, 165, 229  
    bit select 105, 157, 166  
    part select 157, 166

**C**

capacitor model 39  
captured variable 57, 114, 198, 223  
case sensitivity 149  
    Spectre 245  
    SPICE 237  
case statement 201  
charge conservation 54  
Charge nature 159  
circular integrator 75, 179  
clock model 103, 209  
comment 36, 149  
compact model 9  
comparator model 121, 226, 227  
compatibility  
    AMS Designer 248–258  
    Spectre 241–247  
    SPICE 236–241  
    Verilog-HDL 235  
component 46  
concatenate operator 106, 154  
concurrent block 106, 211  
conditional  
    case statement 201  
    if-else statement 68, 200  
    inline 174, 200  
conductor model 39  
configuration 256  
connect module 131–145  
    analog to digital 131  
    automatic insertion 128, 253  
    bi-directional 135  
    digital to analog 135  
connect statement 125, 129, 163  
connectrules 125, 129, 163  
conservative  
    discipline 160  
    system 46  
constant 152  
    expression 172  
    integer 152  
    logic 152  
    mathematical 155

physical 155  
real 153  
strings 154  
vector 154  
constants.vams file 65, 153  
continuous assignment 102, 213  
    delayed 109, 219  
    wreal 111  
continuous domain 160  
continuous-time kernel 196  
contribution statement 38, 60, 169, 198  
    and indirect assignment 172  
    and simultaneous solution 199  
    restrictions 178  
counter model 109, 210, 211  
cross event 67, 72, 206  
    restrictions 178  
    tolerance 81  
current discipline 161  
Current nature 159  
current source model 41  
current, see flow

**D**

d flip flop model 104, 207, 214, 217  
DAC model 87, 111, 223, 224  
DC analysis 177  
ddt operator 40, 179  
    restrictions 178  
ddt\_nature 96  
decade counter model 210  
decimal constant 153  
define statement 151  
defparam statement 233  
delay  
    # 103, 166, 216  
    not allowed in analog process 196  
    @ 104, 216  
    analog (absdelay) 181  
    gate 230  
    inter-assignment 107, 218  
    net 166  
    wait 105, 218  
    not allowed in analog process 196  
delay function (absdelay) 181  
delay measurement model 80  
derivative (ddt) 40, 179  
derived nature 53

- design 2  
 design methodology  
     bottom up 17  
     primitive top down 17  
     rigorous top down 24  
     top down design principles 19  
 difference equations 187  
 digital functions 221  
 digital signal 3  
 digital to analog connect module 135  
 digital to analog converter model 87, 111, 223, 224  
 diode  
     ideal 73  
     junction 54  
 disable statement 210  
 discipline 36, 51, 100, 160  
     resolution 123–128  
         basic 124  
         compatible disciplines 124, 162  
         detailed 127  
         specifying 252  
 disciplines.vams file 37, 159  
 discontinuity function 69, 79, 80, 191  
 discrete domain 160  
 discrete process  
     accessing analog values 118, 225  
     sensitive to analog events 119, 225  
     variable capture 114, 223  
 discrete-event kernel 209  
 discrete-event signal 3  
 display function 192  
 distributions, random 194  
 domain 160  
 driver/receiver segregation 137  
 driver\_... functions 144, 145
- E**  
 e (exponent) 154  
 edge triggered 67, 80, 104, 217  
 electrical discipline 161  
 elements of style 96  
 environment functions 175  
 equality operators 174  
 escaped identifiers 149  
 event  
     above 120, 207  
     analog 67, 72, 78, 204  
         in discrete process 119, 225  
         restrictions 178  
 cross 67, 72, 81, 206  
 delayed assignment 107, 218  
 different in analog process 196  
 discrete 216  
     in analog process 115, 225  
 expression 217  
 final\_step 83, 205  
 initial\_step 78, 92, 205  
 named 217  
 restrictions 83  
 timer 78, 206  
 exclude keyword 55, 158  
 executable specification 23  
 explicit branch 56  
 expression 172
- F**  
 f (fempto) 154  
 fclose function 193  
 fdisplay function 193  
 file  
     constants.vams 153  
     disciplines.vams 159  
 file inclusion 36, 151  
 filter 177  
     absdelay 181  
     ddt 40, 179  
     idt 179  
     idtmod 75, 179  
     laplace 92, 182  
     restrictions 83, 177  
     sampled data 184  
     slew 181  
     transition 79, 180  
     z 184  
 final verification 29  
 final\_step event 83, 205  
 finish function 191  
 finite-state machines 2, 13  
 FIR filter 187  
 fixed-point formulation 169  
 flicker\_noise stimulus 66, 189  
 flow 47, 161, 168  
     probe 61  
     source 62  
 Flux nature 159

- fopen function 193  
for loop 93, 202  
Force nature 159  
forever loop 220  
fork-join block 106, 211  
formal specification 23  
frequency measurement model 110  
from keyword 55, 158  
fstrobe function 194  
function  
    \$abstime 83, 175  
    \$bound\_step 77, 190  
    \$discontinuity 69, 79, 80, 191  
    \$display 192  
    \$driver\_... 144, 145  
    \$fclose 193  
    \$fdisplay 193  
    \$finish 191  
    \$fopen 193  
    \$fstrobe 194  
    \$limexp 57, 188  
    \$monitor 193  
    \$random 194  
    \$rdist\_... 194  
    \$realtime 176  
    \$stop 191  
    \$strobe 84, 192  
    \$temperature 57, 177  
    \$vt 57, 177  
    \$write 193  
above 120, 207  
absdelay 181  
ac\_stim 66, 189  
analog 204  
analysis 175  
cross 67, 72, 81, 206  
ddt 40, 179  
digital 221  
environment 175  
final\_step 83, 205  
flicker\_noise 66, 189  
idt 63, 179  
idtmod 75, 179  
initial\_step 78, 92, 205  
laplace\_... 92, 182  
last\_crossing 81, 188  
logical 175  
mathematical 172, 175  
noise\_table 66, 189  
restrictions 83  
slew 181  
timer 78, 206  
transition 79, 180  
user defined 190  
    analog 204  
    digital 221  
versus task 220  
white\_noise 66, 189  
zi\_... 184
- G**  
G (giga) 154  
gate-level descriptions 229  
generate loop 203  
genvar 84  
    expression 178, 201, 203  
    restricted for loop 84  
    variables 157  
ground 49  
statement 43, 166
- H**  
hardware description language 1  
hexadecimal constant 153  
hierarchical name 72, 232  
discipline 124
- I**  
IC analysis 177  
ideal diode model 73  
ideal opamp model 171  
identifier 149  
identity operators 174  
idt operator 63, 179  
    restrictions 178  
idt\_nature 96  
idtmod operator 75, 179  
    restrictions 178  
ifdef statement 151  
if-else statement 68, 200  
IIR filter 187  
implicit branch 38, 167  
implicit formulation 59, 169  
Impulse nature 159  
include statement 36, 151  
index, vector 105, 157  
indirect assignment 170

and contribution 172  
multiple 171  
inductor model 40  
lossy 88  
initial process 103, 209  
initial\_step event 78, 92, 205  
inout statement 37, 164  
input statement 37, 164  
instantiation 43, 227  
integer  
constants 152  
variables 156  
integral (idt) 179  
integral (idtmod) 75, 179  
inter-assignment delay 107, 218  
interface component 99, 131–145  
automatic insertion 128, 253  
interval measurement model 80  
inverter model 100  
IP reuse 31  
iterator 202, 220

**J**

join-fork block 106, 211  
junction diode model 54

**K**

k (kilo) 154  
kernel 5  
continuous-time 196  
discrete-event 209  
keywords 150  
kinematic disciplines 161  
Kirchhoff's laws 47, 95

**L**

laplace filters 92, 182  
restrictions 178  
last\_crossing function 81, 188  
restrictions 178  
latch model 105, 230  
level triggered 105, 218  
limexp function 57, 188  
restrictions 179  
logic  
constants 152  
discipline 100, 161  
functions 175  
operators 174

values 102, 156  
variables 103, 156  
loop 202, 220  
analog operator restrictions 178  
for 93, 202  
forever 220  
generate 203  
genvar 84  
repeat and while 202  
lossy inductor 88  
lossy transmission line 245

**M**

M (mega) 154  
m (milli) 154  
M... (math constant) 65, 153  
macro 151  
macromodule 226  
magnetic discipline 161  
Magneto\_Motive\_Force nature 159  
mathematical constants 155  
mathematical functions 172, 175  
mechanical stop model 71  
methodology

bottom-up design 17  
primitive top-down design 17  
principles of top-down design 19  
rigorous top-down design 24

mixed-level simulation 21, 27

mixed-signal  
behavior 111  
netlist 121–145  
simulators 5

model  
ADC 84, 118  
barrier 71  
bit stream generator 206  
breakdown warning 208  
capacitor 39  
clock 103, 209  
comparator 121, 226, 227  
conductor 39  
connect module  
analog to digital 131  
bi-directional 141, 146  
digital to analog 135  
counter 109, 210, 211  
d flip flop 104, 207, 214, 217

DAC 87, 111, 223, 224  
frequency measurement 110  
ideal diode 73  
ideal opamp 171  
independent source 41  
inductor 40  
    lossy 88  
inverter 100  
junction diode 54  
latch 105, 230  
mechanical stop 71  
motor 50  
port 65  
quantizer 243  
relay 67, 115  
resistor 35  
RLC 63  
sample and hold 77, 225  
skin effect 88  
Spectre 244, 257  
SPICE 238, 241, 244, 257  
structural 41–50, 121–145, 226–233  
switch (controlled) 67, 115  
time interval measurement 80  
tristate buffer 224  
VCO 73, 118  
modeling plan 22, 24  
modeling style 96  
module 37, 226  
    SPICE 239  
monitor function 193  
motor model 50  
multiple indirect assignment 171  
multiple instantiation 229  
multiplicity factor 241

**N**

n (nano) 154  
name, hierarchical 232  
    discipline 124  
named block 197, 210  
named branch 56, 167  
named event 217  
names, SPICE 239  
nature 36, 51, 95, 159  
negedge 105, 217  
net 164  
    assignment 214

delay 166  
rules of use vs. resistors 215  
signal access 168  
types 165  
vector 164  
versus node 162  
netlist 41–50, 121–145, 226–233  
    definition 45  
node 47, 164  
    versus net 162  
nodeset analysis 177  
noise analysis 66, 177, 189  
noise\_table stimulus 66, 189  
non-blocking assignment 108, 213  
number 152

**O**

octal constant 153  
OOMR 233  
    discipline 124  
opamp, ideal 171  
operator 172  
    analog 177  
    concatenate 106, 154  
    ddt 40, 179  
    idt 63, 179  
    idtmod 75, 179  
    replicate 154  
    restrictions 83, 177  
out of module reference (OOMR) 233  
    discipline 124  
output statement 37, 164  
override, absolute tolerance (abstol) 159

**P**

p (pico) 154  
P\_... (physical constant) 65, 153  
parallel block, see concurrent block  
parameter 37, 55, 75, 157, 228  
part select 157, 166  
physical constants 155  
pin, see port  
plan, verification and modeling 22, 24  
port 37, 46, 164, 228  
    branch 168  
    direction 37, 164  
    model 65  
    signal access 168  
    vector 84, 166

- posedge 105, 217  
 Position nature 159  
 potential 47, 161, 168  
   probe 61  
   source 62  
 primitive  
   Spectre 244, 257  
   SPICE 239, 257  
 probe branch 61  
 procedural assignment 212  
 procedural block 106, 196, 209  
 procedural continuous assignment 214  
 process 38, 103, 196, 209  
   analog 38, 196  
   initial and always 209  
   variable capture 57, 114, 198, 223  
 pseudo-random bit stream generator 206
- Q**  
 quantizer model 243
- R**  
 random function 194  
 range limit 55  
 rdist\_... functions 194  
 real  
   constants 153  
   variables 157  
 realtime function 176  
 real-valued event driven nets 164  
 reduction operators 173  
 reference directions 50  
 reference node 43, 49, 166  
 reg, see register  
 register 103, 156  
   assignment 212, 214  
   captured 198, 223  
   rules of use vs. nets 215  
 register-transfer level 2, 13  
 relational operators 174  
 relative tolerance (reltol) 95  
 relay model 67, 115  
   non ideal 69, 115  
 repeat loop 202  
 replicate operator 154  
 resetall statement 152  
 resistive port model 65  
 resistor model 35  
 resistor noise 66, 189
- resolveto statement 125, 163  
 restricted for loop 84, 203  
 reuse 31  
 RLC model 63  
 rotational disciplines 161  
 rules of scope 230
- S**  
 sample and hold 186  
   model 77, 225  
 scalared 166  
 scale factors 43, 153  
 scaling 96  
 scope rules 230  
 sequential block, see procedural block  
 shift operators 174  
 signal 167  
   attributes, accessing 168  
 signal flow 75  
   discipline 160  
   port 166  
 simulation 1  
   mixed level 21, 27  
   plan 22, 24  
 simultaneous solution 199  
 skin effect model 88  
 slew filter 181  
   restrictions 178  
 small-signal analysis 65  
 source branch 62  
 specification, executable 23  
 Spectre ix, x  
   case sensitivity 245  
   compatibility 241–247  
   from AMS Designer 257  
   model 244  
   subcircuit 245  
   with Verilog-A 241  
 SPICE 8  
   case sensitivity 237  
   compatibility 236–241  
   from AMS Designer 257  
   model 238, 241, 244  
   multiplicity factor 241  
   names 239  
   primitive 239  
   subcircuit 238  
 spontaneous events 78, 206

- state equations 171  
state variable 79  
static analysis 177  
stimulus, ac and noise 66, 189  
stop function 191  
stop, mechanical 71  
string  
    as argument 208  
    constant 154  
strobe function 84, 192  
structural module 41–50, 121–145, 226–233  
    definition 45  
style, modeling 96  
subcircuit  
    Spectre 245, 257  
    SPICE 238, 257  
supply0, supply1 wire types 165  
switch (controlled) model 67, 115  
    non ideal 69, 115  
switch branch 62, 169  
synchronization  
    analog event in discrete process 120  
    discrete event in analog process 116  
synthesis 1, 13  
system 46  
system function, see function  
system-level verification 26  
SystemVerilog ix, 249
- T**  
T (tera) 154  
task 221  
    versus function 220  
temperature function 57, 177  
Temperature nature 159  
terminal, see port  
test 30  
test bench 10  
thermal discipline 161  
thermal noise 66, 189  
thermal voltage (vt) function 177  
time function 83, 175, 176  
time interval measurement model 80  
time unit 152, 176, 216, 218  
timer event 78, 206  
timescale 152  
timing control 104, 216  
tolerance 94
- see absolute tolerance  
see relative tolerance  
top-down design methodology  
    primitive 17  
    principles 19  
    rigorous 24  
top-level module 227  
torque nature (Angular Force) 52, 159  
transient analysis 177, 242  
transition filter 79, 180  
    restrictions 178  
transmission line 245  
tri, triand, trior, tri0, tri1, trireg wire  
    types 165  
triggered  
    edge 67, 80, 104, 217  
    level 105, 218  
tristate buffer model 224
- U**  
u (micro) 154  
unary reduction operators 173  
undef statement 151  
units 52, 159  
unnamed branch 38, 167  
user-defined functions 190  
    analog 204  
    digital 221
- V**  
variable 57, 155  
    captured 57, 114, 198, 223  
genvar 157  
initialization 57  
integer 156  
logic 103, 156  
real 157  
register 103, 156  
vector 105  
    vectors 157  
VCO model 73, 118  
vector 157  
    access 105, 157  
bit select 105, 157, 166  
branch 167  
constants 154  
instance 229  
net 164  
part select 157, 166

port 84, 166  
 see bus  
 variables 105, 157  
 vectored 166  
 Velocity nature 159  
 verification  
     bottom up 28  
     final 29  
     mixed level 21, 27  
     plan 22, 24  
     system level 26  
 Verilog languages 2  
 Verilog-A 35–98  
     with Spectre 241  
 Verilog-HDL compatibility 235  
 VHDL-AMS 2, 257  
 voltage discipline 161  
 Voltage nature 159  
 voltage source model 41  
 voltage, see potential  
 VPI 234  
 vt function 57, 177

**W**

wait 218  
     not allowed in analog process 196  
 wait statement 105  
 wand (wired and) wire type 165  
 while loop 202  
 white\_noise stimulus 66, 189  
 wire 101, 165  
 wor (wired or) wire type 165  
 wreal wire type 164  
 write function 193

**X**

x logic value 101, 102, 153, 156  
     accessing in analog process 223, 224

**Z**

z filters 184  
     restrictions 178  
 z logic value 101, 102, 153, 156  
     accessing in analog process 223, 224