

ASIC/SoC Documentation – Controlling Device Costs

Scott Meltzer
SF Group, Inc.

Version 1, 6 November 2007

Your customers design their systems based on preliminary documentation, weeks or even months before your IC product is silicon. Incorrect, incomplete, or confusing product information published at the preliminary stage can be very costly to you and your customer.

This document addresses (in some cases introduces) the basics of ASIC documentation requirements and provides some insight into how to reduce device time-to-market.

Last updated on February 15, 2008. You can find the most recent version at www.designers-guide.org. Contact the author via e-mail at scottmeltzer@sfgroup-inc.com. The author has worked for a number of semiconductor companies (Intel, Philips Semiconductors, National Semiconductor), is president of SF Group, Inc., a documentation outsourcing service provider, and a member of the Society for Technical Communication (STC).

Permission to make copies, either paper or electronic, of this work for personal or classroom use is granted without fee provided that the copies are not made or distributed for profit or commercial advantage and that the copies are complete and unmodified. To distribute otherwise, to publish, to post on servers, or to distribute to lists, requires prior written permission.

1 Introduction

Not long ago, simple two- to four-page datasheets were sufficient for most semiconductor devices. These documents could be generated quickly and cheaply. Mainly used as product brochures, these were given very little attention by device manufacturers.

Modern datasheets are really design guides, not just AC and DC characteristics or maximum operating conditions. ASIC/SoC datasheets are cookbooks that are required in order for a chip customer to be able to implement any or all of a device’s feature set.

This shift in the requirements and the importance of the datasheet has gone largely unnoticed by semiconductor industry, especially in the fabless community.

However, a census concern, from IDMs to fabless companies is: controlling device costs. Yet most companies overlook one of the biggest reasons for rising device costs.

Compilation of poll results of executives and engineers quite clearly show that chip documentation is not among the top reasons given for escalating device costs. When in fact, the costs for producing the device documentation is a major reason for going over budget.

This paper addresses (in some cases introduces) the basics of ASIC documentation development and provides some insight into reducing device costs and possibly time-to-market.

2 Chip Documentation

Unlike other technology products, whose success or failure isn’t necessarily linked to the quality of its documentation, an ASIC/SoC product’s success is largely due to the accuracy, completeness, and organization of its preliminary documentation.

A quick review of Table 1 illustrates the important distinctions between the documentation requirements for ASIC/SoC products versus other high-tech products.

TABLE 1 *Crucial differences between semiconductor documentation vs. other high-tech products.*

Requirement	ASIC/SoC	Other Products
Required prior to first customer ship?	Yes	No
Sale dependant on documentation?	Yes	No
Sale dependant on accuracy/completeness/organization of documentation?	Yes	No
Deadline required?	Yes	No
Actually used?	Yes	Maybe
Actually useful?	Yes	Possibly

The reason for such a disparity is simple: ASIC/SoC product documentation (referred to as “datasheet” in this paper) is documentation for a product that doesn’t even exist yet. Another reason is that other high-tech companies are simply not compelled to create useful, usable product documentation.

This non-standard situation requires a non-standard solution in order to avoid the inevitable: scrambling around at the last minute in an attempt to put together adequate documentation upon which the sale is probably dependent.

3 Datasheet Standards

For ASIC companies, the most widely-read documents they publish will probably be their product datasheets. Chip customers can form lasting impressions of ASIC companies based solely on the “look and feel” and content of device datasheets. Inaccurate, unorganized, and “ugly” datasheets can disqualify a well-designed device, especially when customers have a choice of device manufacturers.

Over the years the semiconductor industry has adopted a de-facto standard to address some of these weaknesses, specifically with regards to the organization of datasheets. In most datasheets you will find these sections:

- General Information
- Key Features
- Electrical Characteristics
- Detailed Description
- Application Examples
- Ordering Information

This presents an organized and “branded” look, and will probably satisfy the chip customer’s basic needs. Basic being the operative word.

Chip designers are well familiar with the shortcomings of their device’s datasheets, and usually these shortcomings are due to the datasheet only meeting the basic needs of the customers. Meeting basic needs will not somehow magically eliminate the frequent telephone calls from customers in need of support for the device.

4 Datasheet Requirements

Datasheets that conform to the de-facto industry standard are probably not going to empower a chip customer to be self-supportive when implementing an ASIC device.

Why not? Five simple, yet important reasons:

4.1 Accuracy

Mistakes, especially in parametric data can kill a sale (and oftentimes a product). Names (pin/pad/ball/register/bit) are where most datasheet mistakes are found. Whether this is due to product evolution, intentional name changes, legacy name remnants, and so on, this problem can be resolved by a deploying a documentation development process.

Fact checking and verification simply do not exist in most datasheet development processes (assuming there actually are development processes), and can be accomplished by skilled technical writers with the right tool (see “Authoring Tool Selection” on page 7.).

4.2 Completeness

Information that is missing, or misplaced (even redundant) can be a major reason for the rejection of devices by chip customers.

For today's ASICs, datasheet completeness can be the sole reason for getting or losing the sale.

Additionally, an incomplete datasheet in the chip customer's hands means someone is going to be on the phone supporting the customer, post sale. And that same someone will probably be required to develop tomorrow's products in between phone calls.

Redundant information can be one of the biggest sources of confusion when designing against a device datasheet. Most chip designers are not professional writers. They write fast and frequently. And have been known to repeat themselves in text intended for datasheets (on occasion). And, since most chip designers are the sole "owners" of their devices, it is quite understandable that he/she becomes so intimately involved with the datasheet that redundancy is very often not "seen".

4.3 Organization

The datasheet should have everything known about the chip arranged in such a way as to make locating this information as easy as possible.

An unambiguous explanation of the device cannot be achieved without careful consideration of the organization. Whether this be done using hyperlinks or careful design, datasheet content *must* flow in an orderly manner in order to be considered useful.

4.4 Costs

There is traditionally not a good solution to keeping documentation costs under control. This is especially true in the semiconductor industry.

The reasons for not being able to control costs lie somewhere in the development of the documentation. The reasons are many and varied.

Of course there are other factors which increase documentation costs, but those are normally due to feature changes, project hand-off, management decisions, and so on, and are not caused by the documentation development itself.

Note: *As the costs of ASIC device development typically include the costs for the associated documentation, when we talk about controlling documentation development costs, what we are really talking about is controlling device development costs.*

4.5 Timeliness

Many ASIC customers are ready to design their system around a chip weeks or months before the device has even begun the characterization stage. Having a partially completed or unorganized datasheet at this stage will most likely negatively affect a chip customers evaluation of a device.

Everyone knows of a particular sale that was lost due to an incomplete, inaccurate, or non-existent datasheet. Modern devices require preliminary datasheets, and released

datasheets must be updated frequently, with the most current data available to the customer.

4.6 Requirements Summary

For whatever reason, and this is more likely to be true in fabless companies, these 5 requirements are rarely factored into chip documentation development, for even the most sophisticated devices.

Probably some are, but not all.

For modern devices to meet today's ever-shrinking time-to-market deadlines, the associated datasheets must meet certain requirements which go beyond the de-facto datasheet standard.

5 Controlling Costs

Standard methods used to attempt to control documentation costs are:

Hire a technical writer. This is a risky gamble for several reasons: the unknown-less of the technical writer (does he know what he is doing/supposed to be doing, will she be able to do it, will they still be here tomorrow?); the unknown-less of the cost-per-datasheet (how long/much will it take to produce the datasheet's preliminary release; subsequent releases?).

Use a staffing agency. Anyone who has tried this knows this is really a trick option, in that it is worse, economically speaking, than the first option. Staffing agencies routinely demonstrate that they do not understand their clients' needs¹. For the semiconductor industry this is critically important, with time-to-market schedules shrinking at rates closing in on Moore's law.

6 Cost Increase Contributors

Take the case for an "average" 100-page datasheet. Using the industry average of 4 pages-per-hour (production) and labor-rates of \$40/hour (hired-staff) and \$80/hour (staffing agency), a 100-page datasheet will take the average technical writer 400 hours to produce the initial release, and cost \$16,000 done by hired-staff² and a whopping \$32,000 when using a staffing agency.

This "cost" does not include the following cost-increase contributors:

- Costs to develop a productive documentation development process (DDP).
- Considerations that, without a productive DDP, the estimated time of 400 labor-hours could increase by as much as double.
- Re-work due to an ineffective DDP, engineering changes and/or marketing requirement changes.

-
1. Based on the author's observations working for such agencies and interviews with agency clients.
 2. This does not reflect initial hiring costs and other expenses related to full-time employment.

- Re-work caused by human or computer errors³.
- Re-work caused by inexperienced datasheet authors⁴.

Using the traditional (word-processing) approach, the total actual costs for this average 100-page data sheet can be as high as \$60,000!⁵

It's no wonder the mere mention of the word datasheet causes CFOs to cringe and search for cheaper alternatives.

7 The Data Sheet Dilemma

Companies who purchase large quantities of ASIC devices (chip customers – such as mobile phone, laptop, and a portable-device manufacturers) design their systems based on preliminary documentation, weeks or even months before an ASIC product is silicon.

Incorrect, incomplete, or confusing product information published at the preliminary stage can be very costly to the ASIC manufacturer and their customers.

More than a few ASIC device projects have been abandoned simply due to the lack of, or unusable documentation.

Most of the time this is due to writers who are not familiar with the semiconductor industry having been assigned to create the datasheet. This has proven to be an unsuccessful formula time and again.

As a non-standard approach to ASIC documentation development is required, the question becomes:

“How do I get my datasheets done in a timely manner, will not cost my company a small fortune, are accurate, complete, and organized, and will win over my customer?”

8 A Solution

The answer is: **preparation.**

In order to avoid putting incomplete, inaccurate, or immature datasheets into the chip customer's hands, some process(es) must be established and sponsored by management. For ASIC companies, this must be given even more consideration due to the importance of meeting time-to-market deadlines.

8.1 Documentation Development Process (DDP)

The best (read: smartest) way to satisfy both the de-facto standard and the additional datasheet requirements is to process-size datasheet development. This means establishing standards for the documentation's “look and feel”, developing datasheet-creation

-
3. This cost-increase contributor is particularly difficult to control, and essentially is the subject of this paper.
 4. This contention is based on the author's observations and interviews with chip designers.
 5. In the author's opinion, using familiar, non-long-document tools will mostly likely increase this figure by 30%.

and -update procedures, and giving the documentation the support and attention worthy of its importance to the sale of the associated device.

8.1.1 Functions

A well-designed DDP should include considerations for the following:

- Creation and deployment of a stable and useful documentation template; an under-featured template equates to more labor hours per datasheet.
- Key data-validation methods; pin/pad/ball/register/bit names must be verified and rogue names removed. Product variants and model numbers also fall into this category.
- Consistency checks for technical terms (e.g., step-down, buck, converter). This is a key source of confusion in technical documentation, especially in the ASIC industry.
- Reliable cross-reference and hyperlink mechanisms; broken or invalid links are useless.
- Provides for organization, completeness, and redundancy checks; confusing, misleading, or incomplete datasheets live a very short life.
- Methods for creating device-specific technical diagrams and illustrations; a library of standard symbols is required. As for package drawings and timing diagrams, these should be treated as content and handled in the same manner. See “DPP Benefits” on page 8.

8.1.2 Authoring Tool Selection

It’s no secret that the tool-of-choice can delay datasheet development, and possibly customer acceptance of an ASIC. It is vitally important that the datasheet development schedule never be compromised by the capabilities of the authoring tool.

Long documents such as an ASIC datasheet will simply overwhelm word-processors like Word or Word Perfect. Long document management requires a long-document tool such as Framemaker (the tool-of-choice of major IDMs as well as a growing number of fabless companies).

Many of the DDP requirements, such as data-validation, reliable cross-referencing, and so on, can only be achieved by a long-document application. If any single component required for the production of quality, usable datasheets can be identified, it would be the authoring tool. It just makes good business sense: the right tool for the job.

8.1.3 Technical Writer Selection

With regards to finding the right technical writer there simply is no easy answer for this, however you can educate yourself on what you should expect from the writer.

Most technical writers outside of the semiconductor industry, while familiar with tight schedules, are not aware of the importance of timely and accurate documentation completion in the semiconductor industry. This is because most other industries change their production or delivery schedules for a variety of reasons, and the urgency to deliver on-time simply isn’t there, company-wide. Certainly this has a trickle-down effect “down” to and including the technical writer.

Many come from large companies with behemoth systems in place, which naturally leads to inefficiency and indifference. And baggage.

To create usable datasheets for modern ASIC devices, the following characteristics of the technical writer are mandatory:

- English writing/editing expertise
- IC product information experience
- Long-document application power-user
- Native-English speaker
- Engineer-Friendly

8.2 DPP Benefits

A summary of the main benefits of investing in a documentation development follows:

- Can satisfy the datasheet requirements (see “Datasheet Requirements” on page 3).
- The appropriate long-document application, when used with a functional template, can result in reduced production times by anywhere from 20- to 50-percent versus the traditional approach. Additionally, more realistic documentation schedules can be made. And met.
- An integral part of the DDP is the concept of management sponsorship. This means someone (not the writer) MUST take ownership of the datasheet – usually the chip designer – and this person must have the support of upper management and empowered to make decisions.
- A seamless and fluid flow of information from the engineer to the technical writer is the only way to ensure accuracy is maintained and up-to-date. A haphazard approach will (not probably) result in cost increases due to re-work. This should include not only original source material, but also a means to provide information uncovered during device development on an ongoing basis.
- Volumes can be written on the importance of clarity and organization (see “Organization” on page 4). One of the few negative aspects of the aforementioned “datasheet standards”, is the idea that merging separate ideas into giant paragraphs is useful. It isn't. Information must be broken down into bite-sized pieces, especially when application information is concerned.
- Datasheet information must be clear, concise, and to the point, again especially application information. Chip customers rely heavily on the “usability” and “readability” of device datasheets.
- Datasheet production can and should be done in parallel with device development. However, with a well-designed DDP, the datasheet development will advance at a much more rapid pace, enabling preliminary releases to be sent to chip customers earlier.
- Once the preliminary release has been delivered, frequent and regular updates can be made available to the customer thanks to the DDP.
- Data re-use. Many times data is reusable, say for an associated document such as a Product Brief, or a device in a specific family. This is frequently a cost-increase contributor that can be resolved with a well-designed DDP.

9 Conclusion

Controlling ASIC development costs are critical to the success of ASIC devices and their respective companies.

A leading contributor to budget increases is the oftentimes uncontrollable costs of the documentation.

With a well thought-out documentation development process, the right authoring tool, and a technical writer with knowledge of the semiconductor industry, documentation costs can be controlled, and ASIC sales need no longer rely so crucially on the associated documentation.